AMENDMENTS TO THE CLAIMS:

Please cancel claims 7, 12, 39, and 40 without prejudice or disclaimer and amend the claims as follows:

1. (Currently Amended) A double-gate field effect transistor, comprising:

a strained-silicon channel formed adjacent a source and a drain on a substrate, said strained-silicon channel comprising two separated portions, wherein each of said two separated portions of said strained-silicon channel connects said source and said drain;

a first gate formed over a first vertical outer side of said strained-silicon channel;

a second gate formed over a second vertical inner side of said strained-silicon channel located between said two separated portions of said strained-silicon channel;

a first gate dielectric formed between said first gate and said strained-silicon channel; and

a second gate dielectric formed between said second gate and said strained-silicon channel,

wherein said strained-silicon channel is non-planar, said first gate comprises at least one chemical element not included in said second gate, said first gate dielectric is chemically different than said second gate dielectric.

2. (Currently Amended) The double-gate field effect transistor of claim 1, wherein said strained-silicon channel thickness is substantially uniform.

3. (Currently Amended) The double-gate field effect transistor of claim 1, wherein said strained-silicon channel thickness is set by epitaxial growth.

4. (Currently Amended) The double-gate field effect transistor of claim 1, wherein said strained-silicon channel is substantially defect-free.

5. (Currently Amended) The double-gate field effect transistor of claim 1, wherein said strained-silicon channel includes a distorted lattice cell.

6. (Currently Amended) The double-gate field effect transistor of claim 1, wherein said first gate and said second gate are independently controllable.

7. (Canceled)

8. (Currently Amended) The double-gate field effect transistor of claim 1, wherein said first gate and said second gate are self-aligned.

9. (Currently Amended) The double-gate field effect transistor of claim 1, wherein said first gate and said second gate are defined in a single lithographic step.

10. (Currently Amended) The double-gate field effect transistor of claim 1, wherein said first gate, said second gate, said source and said drain are self-aligned with respect to each other.

11. (Currently Amended) The double-gate field effect transistor of claim 7, further comprising a plurality of fins.

12. (Canceled)

13. (Canceled)

14. (Canceled)

15. (Canceled)

16. (Canceled)

17. (Canceled)

18. (Canceled)

19. (Canceled)

20. (Canceled)

21. (Currently Amended) A double-gate field effect transistor, comprising:

a strained-silicon channel formed adjacent a source and a drain on a substrate, said strained-silicon channel comprising two separated portions, wherein each of said two separated portions of said strained-silicon channel connects said source and said drain;

a first gate formed over a first vertical outer side of said strained-silicon channel;

a second gate formed over a second vertical inner side of said strained-silicon channel located between said two separated portions of said strained-silicon channel;

a first gate dielectric formed between said first gate and said strained-silicon channel; and

a second gate dielectric formed between said second gate and said strained-silicon channel,

wherein said strained-silicon channel comprises fins, said first gate comprises at least one chemical element not included in said second gate, said first gate dielectric is chemically different than said second gate dielectric. ~~a fin.~~

22. (Previously Presented) A circuit, comprising:

the double-gate field effect transistor of claim 1.

23. (Currently Amended) The double-gate field effect transistor of claim 1, wherein said strained-silicon channel is tensely strained.

24. (Currently Amended) The double-gate field effect transistor of claim 1, wherein said strained-silicon channel is compressively strained.

25. (Canceled)

26. (Canceled)

27. (Canceled)

28. (Currently Amended) The double-gate field effect transistor of claim 1, wherein the first gate is electrically separated from the second gate.

29. (Currently Amended) The double-gate field effect transistor of claim 21, wherein the first gate is electrically separated from the second gate.

30. (Currently Amended) A semiconductor device, comprising:

a strained-silicon channel formed adjacent a source and a drain on a substrate, said strained-silicon channel comprising two separated portions, wherein each of said two separated portions of said strained-silicon channel connects said source and said drain;

a first gate formed over a first vertical outer sidewall of said strained-silicon channel;

a second gate formed over a second vertical inner sidewall of said strained-silicon channel located between said two separated portions of said strained-silicon channel;

a first gate dielectric formed between said first gate and said strained-silicon channel; and

a second gate dielectric formed between said second gate and said strained-silicon channel,

wherein said strained-silicon channel is non-planar, and said first vertical outer sidewall and said second vertical inner sidewall ~~first and second sidewalls~~ are opposing to

each other, said first gate comprises at least one chemical element not included in said second gate, said first gate dielectric is chemically different than said second gate dielectric.

31. (Currently Amended) A semiconductor device, comprising:

a strained-silicon channel formed adjacent a source and a drain on a substrate, wherein strain in said strained-silicon channel was elastically induced by a sacrificial stressor said strained-silicon channel comprising two separated portions, wherein each of said two separated portions of said strained-silicon channel connects said source and said drain;

a first gate formed over a first vertical outer side of said stained-silicon channel;

a second gate formed over a second vertical inner side of said strained-silicon channel located between said two separated portions of said strained-silicon channel;

a first gate dielectric formed between said first gate and said strained-silicon channel; and

a second gate dielectric formed between said second gate and said strained-silicon channel,

wherein said strained-silicon channel is non-planar, and is fixed to the substrate by said first and second gates, said first gate comprises at least one chemical element not included in said second gate, said first gate dielectric is chemically different than said second gate dielectric.

32. (Currently Amended) The double-gate field effect transistor of claim 1, wherein strain in said strained-silicon channel was elastically induced by a sacrificial stressor.

33. (Currently Amended) The double-gate field effect transistor of claim 21, wherein strain in

said strained-silicon channel was elastically induced by a sacrificial stressor.

34. (Currently Amended) The double-gate field effect transistor of claim 1, wherein said strained-silicon channel is controlled by said first gate and by said second gate.

35. (Currently Amended) The double-gate field effect transistor of claim 21, wherein said strained-silicon channel is controlled by said first gate and by said second gate.

36. (Currently Amended) The double-gate field effect transistor according to claim 1, wherein said first gate and said second gate are separated from one another.

37. (Currently Amended) The double-gate field effect transistor according to claim 1, wherein carriers in said channel are controlled by said first gate and said second gate.

38. (Currently Amended) The double-gate field effect transistor according to claim 1, wherein said strained-silicon channel comprises [[a]] first vertical outer side ~~surface~~ covered by said first gate dielectric and [[a]] second vertical inner side ~~surface~~ covered by said second gate dielectric.

39. (Canceled)

40. (Canceled)

41. (Currently Amended) The double-gate field effect transistor according to claim 1,

wherein a thickness of said first gate dielectric is independent of a thickness of said second gate dielectric.

42. (Currently Amended) The double-gate field effect transistor according to claim 1, further comprising a fixing material disposed under said second gate.

43. (Currently Amended) The double-gate field effect transistor according to claim 21, further comprising oxide plugs formed over said fins. ~~fin.~~